designideas

READERS SOLVE DESIGN PROBLEMS

Circuit compensates system offset of a load-cell-based balance

Luca Bruno, ITIS Hensemberger, Monza, Italy

It's a challenge to interface a resistive bridge sensor with an ADC receiving its power from a 5V single-supply power source. Some applications require output-voltage swings from 0V to a full-scale voltage, such as 4.096V, with excellent accuracy. With most single-supply instrumentation amplifiers, problems arise when the output signal approaches 0V, near the lower output-swing limit of a single-supply instrumentation amp. A good single-supply instrumentation amp may swing close to single-supply ground but does not reach ground even if it has a true rail-to-rail output.

In this application, the sensor is a precision load cell with a nominal load of 5 kg, or about 11 lbs, to weigh objects on an aluminum pan weighing approximately 150g, or approximately 5 oz. Because of the pan's weight, the instrumentation amplifier's output signal can never go down to 0V, even if there are no objects to weigh. Now, the problem arises of how to compensate the instrumentation amp's output-offset voltage and the voltage that the pan itself produces.

A software approach is the simplest way to compensate the system offset. During power-up, there are no objects to weigh on the pan, and the system can thus acquire the offset voltage and hold the data in the microcontroller's memory, subsequently subtracting it from the data it acquired when there was an object to weigh. This approach, however, does not reach the 5-kg full-scale of the balance, reaching only 5−0.15 kg, or 4.85 kg.

This Design Idea shows how to achieve hardware compensation us-

▶What are your design problems and solutions? Publish them here and receive $150! Send your Design Ideas to edndesignideas@reedbusiness.com.
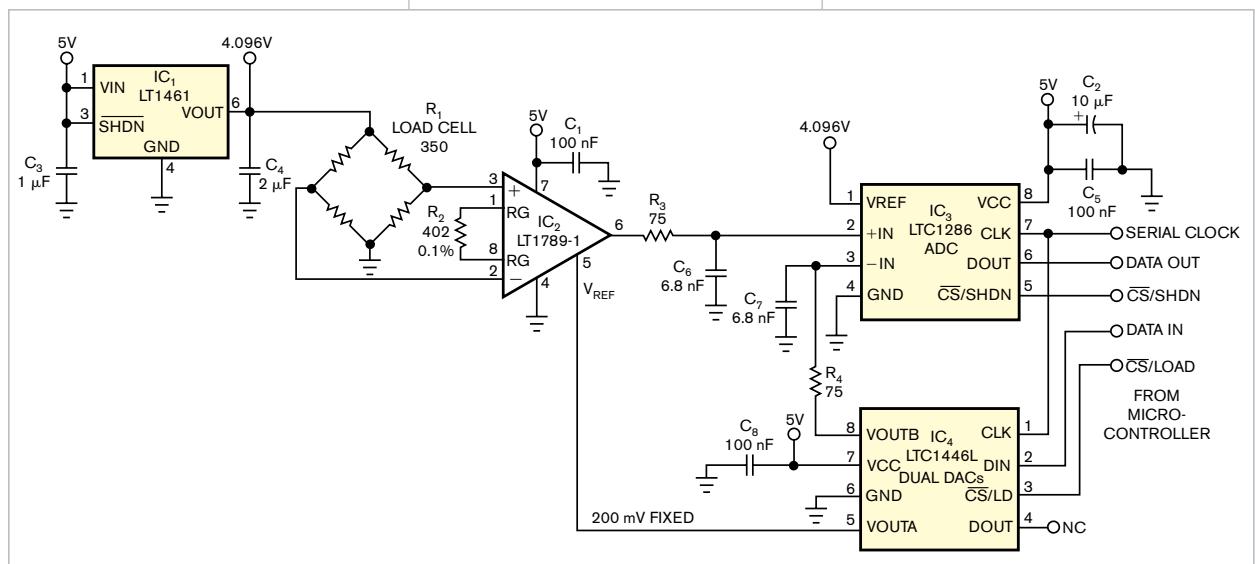

Figure 1 The serial dual DAC in this circuit gets an offset voltage from the microprocessor (not shown) during a power-on-calibration routine.

ing a microcontroller that, on power-up, starts a software routine to reset the system offset. The solution is a simple circuit based on four ICs from Linear Technology (www.linear.com) in **Figure 1**. A precision voltage reference, IC_1, has a high minimum output current of 50 mA. It provides an output voltage of 4.096V to power the load cell and to set the full-scale of the 12-bit ADC, IC_3. The highly accurate LT1789-1 instrumentation amplifier, IC_2, features maximum input-offset voltage of 150 μV over the temperature range of 0 to 70°C and maximum input-drift-offset voltage of 0.5 μV/°C over the temperature range of 0 to 70°C with rail-to-rail output that swings within 110 mV of ground. You set the gain through precision resistor R_2 to a nominal value of 500Ω to give an output span of 4.096V when the load is 5 kg and its maximum input signal is $V_{CC} \times S = 4.096V \times 2$ mV/V=8.192 mV, where S is the sensor's sensitivity.

The output of DAC_A of dual-DAC IC_4 provides a reference voltage of 200 mV at the reference pin of the instrumentation amp to avoid saturation near ground of the amplifier itself, where its transfer characteristic is not quite linear. The amplifier's total worst-case output offset is: $V_{REF} + V_{PAN} \pm V_{OFFSET} = 200$ mV+125 mV±500×150 μV=325 mV±75 mV=250 mV/400 mV, where $V_{PAN} = 125$ mV and is the voltage that the pan's weight produces.

The system-output offset is thus 250 to 400 mV. On power-up, the microcontroller starts a routine that sets the output of the DAC_A equal to 200 mV, while it increases the output of the DAC_B of dual-DAC IC_4 until it is equal to the system offset on Pin 2 of ADC IC_3, and the result of the conversion is 000h. This result is possible because IC_4 contains two 12-bit DACs with the same full-scale voltage of 2.5V, making 1 LSB equal to 0.61 mV, which is smaller than IC_3's resolution of 1 mV. This figure corresponds to the resolution of the balance: 5000g/4096=1.22g. The maximum output voltage of the instrumentation amp with a maximum load of 5 kg is $4.096V + V_{OUT\_TOTAL\_OFFSET\_INA} = 4.346V/4.496V$, which is less than the minimum worst case over temperature of 4.62V high saturation.

IC_3 has a single unipolar differential input, so you can subtract from the +IN input voltage a constant voltage of value equal to the system offset that that DAC_B of IC_4 provides. During the first one and a half clock cycles, the ADC samples and holds the positive input. At the end of this phase, or acquisition time, the input capacitor switches to the negative input, and the conversion starts. The RC-input filters on the inputs of IC_3 have a time constant of 0.5 μsec to permit the negative and positive input voltages to settle to a 12-bit accuracy during the first clock cycle of the conversion time, using the maximum clock frequency, which is 200 kHz. If you want to increase the time constant, then you must use a lower clock frequency.

Furthermore, the DAC and ADC have a three-wire serial interface that easily permits transferring data to a wide range of microcontrollers with a maximum sampling rate of 12.5k samples/sec. When the ADC performs no conversions, it automatically powers down to 1 nA of supply current, and, if the microcontroller shuts down IC_1 through its Pin 3, the circuit draws a worst-case supply current of just 1 mA, because all the ICs are micropower.**EDN**
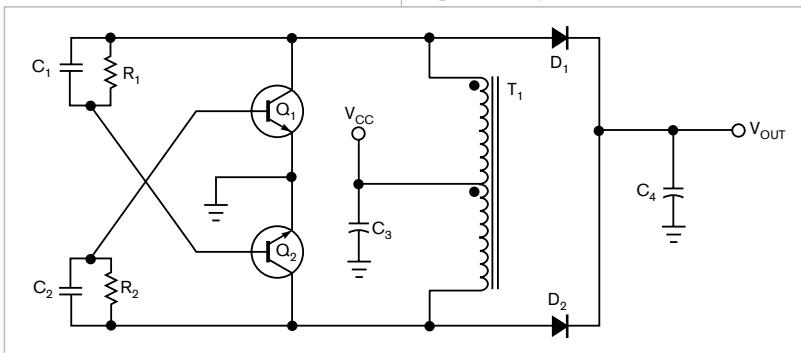
Voltage doubler uses inherent features of push-pull dc/dc converter

Ajoy Raman, Aeronautical Development Establishment, Bangalore, India

This Design Idea presents a minimal-parts-count, wide-range voltage doubler using the inherent voltage-doubling characteristics of a one-transformer push-pull dc/dc converter. The implementation uses a high-voltage Darlington-array driver, ULN2023A. The circuit exhibits a wide input-voltage range of 5 to 30V and provides a typical power output of 1 to 4W at moderate efficiency.

Figure 1 shows a simple, one-transformer dc/dc converter in which cross-coupled RC networks from the collectors of Q_1 and Q_2 to the corresponding bases provide regenerative feedback. In operation, the transformer alternates between positive and negative saturation, with collapse in transformer flux leading induced voltages to drive the transistors alternately off and on. The input-voltage and saturation charac-

Figure 1 A simple one-transformer dc/dc voltage doubler has cross-coupled RC networks from the collectors of Q_1 and Q_2 to the corresponding bases. These networks provide regenerative feedback.

TABLE 1 EXPERIMENTAL RESULTS

Input voltage (V)	Input current (mA)	Oscillating frequency (kHz)	Output voltage (V)	Load current (mA)	Power input (W)	Power output (W)	Efficiency (%)
5	245	1.79	7.59	105.95	1.22	0.8	65.77
10	250	4	17.68	104.13	2.5	1.84	73.72
15	274	6.06	27.7	111.7	4.12	3.09	75.08
20	280	8.2	37.9	110.12	5.6	4.17	74.53
25	242	10.53	48.1	88.23	6.05	4.24	70.15
30	205	13.33	58.7	66.25	6.15	3.89	63.23

Figure 3 Taking advantage of the multiple drivers in one package, three drivers are parallel in each leg of the circuit.

Figure 4 Experimental results show the circuit in Figure 3 operating as a low-power, moderately efficient, wide-range voltage doubler.

Figure 2 The internal configuration of the high-voltage Darlington-array ULN2023A driver exactly matches the requirements of the circuit in Figure 1 by providing rectifier diodes at the collector outputs.

teristics of the transformer core determine the operating frequency based on the relationship

$$f = \frac{V_{CC} \times 10^8}{4\beta_S AN} \, Hz,$$

where V_{CC} is the input voltage, β_S is the saturated flux density in gauss, A is the cross-section area of the core in square centimeters, and N is the number of turns in half of the primary. The circuit uses the property that the collector-to-emitter voltage of each device is approximately twice the supply voltage, V_{CC}, plus induced voltages, which occur because of leakage inductance. Rectification and filtration of the collector voltages of Q_1 and Q_2 through D_1 and D_2 directly provide an output voltage that is approximately double the input voltage, V_{CC}.

The internal schematic of the high-voltage Darlington-array ULN2023A driver in **Figure 2** exactly matches the requirements for the circuit in **Figure 1** by providing rectifier diodes at the collector outputs. The voltage-breakdown specification of 95V meets the maximum requirement of twice V_{CC} plus transients when operating at an input of 30V. The device exhibits a low collector-to-emitter saturation voltage at the desired current level of approximately 100 mA and low switching times when switching at rates as high as tens of kilohertz.

Figure 3 shows the final circuit configuration. Three drivers operate in parallel, sharing the drive current, minimizing the collector-to-emitter

voltage, and maximizing the permitted power dissipation. **Table 1** shows the experimental results with the voltage-doubler circuit operating over the input voltage of 5 to 30V. In that range, the input current is less than 300 mA to remain within the current values of the transformer at lower input voltages and within the power-dissipation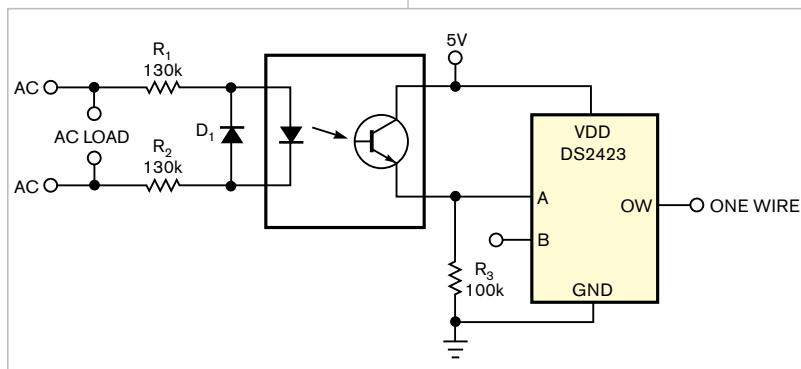 limit of the ULN2023A at higher input voltages. **Figure 4** shows the plot of the experimental results, clearly indicating the operation of a low-power, moderately efficient, wide-range voltage doubler.EDN

Voltage timer monitors line-connected ac loads

Michael Petersen, Maxim Integrated Products, Sunnyvale, CA

A simple circuit monitors the elapsed time over which a line-connected ac load energizes (**Figure 1**). You can then access the elapsed-time count over a standard one-wire protocol. When you energize the ac load, the optoisolator provides pulses at the ac-line frequency to the input of the one-wire counter, a DS2423 IC. Thus, the counter continuously increments whenever you energize the load. Resistors R_1 and R_2 limit the current, and diode D_1 protects the optoisolator from reverse-polarity voltages during the negative half of the line cycle.

As an example, the circuit can monitor the duration of operating intervals for a 240V-ac well pump, thereby giving an indirect measure of the amount of water the well pumps and the approximate amount of power it consumes. The one-wire master counter—a Linux-based PC, for example—reads the elapsed count once per minute. Any change in the count from one reading to the next indicates that the pump is energized and running, and you calculate the length of time in seconds by simply taking the difference in counter values divided by the line frequency—60 Hz, in this case. The time in seconds equals the new count minus the old count divided by 60 Hz.

The circuit can monitor a water heater, a furnace, an air-conditioning unit, or any other ac-connected load. You may need to adjust the R_1 and R_2 values to accommodate line voltages other than 240V ac or the characteristics of other optoisolators. You can also monitor two independent loads by attaching a second optoisolator circuit to the Counter B input of a single DS2423.EDN

Figure 1 This circuit monitors line-connected ac loads by counting one pulse per cycle when the load is energized.

Cascaded converter boosts LED-drive capability

Grant Smith, National Semiconductor, Phoenix, AZ

Powering 20 to 30 white LEDs from three alkaline cells presents an interesting problem for the conventional boost converter. The required boost ratio and duty factor are simply impractical. If you are determined to design with off-the-shelf components, cascading two stages of boost can yield reasonable results. This topology has been around for decades, but engineers often perceive it as too complicated. There are, however, certain inherent advantages in this approach's component requirements. The first-stage switch need not tolerate the total output voltage of the second switch, and the second switch does not have the current requirements of the first. If the duty factor were not a concern, the current/voltage requirements of a single-stage boost would require a larger, more expensive switch that might easily approach the cost of both switches in the cascaded boost. You can also realize similar advantages of the inductors, rectifiers, and filter capacitors.

This Design Idea powers 24 white or ultraviolet LEDs in series at approximately 20 mA. At a nominal 4.5V-dc input, the measured efficiency is 84.2%. This figure is reasonable for a 2 to 2.5W converter. At a 3V-dc input, the overall boost ratio for a noncascaded converter is potentially more than 30-to-1, requiring an on-time duty factor of approximately 97%. In a cascaded boost converter, this duty factor is a function of the square root of the total boost ratio. This ratio equates to
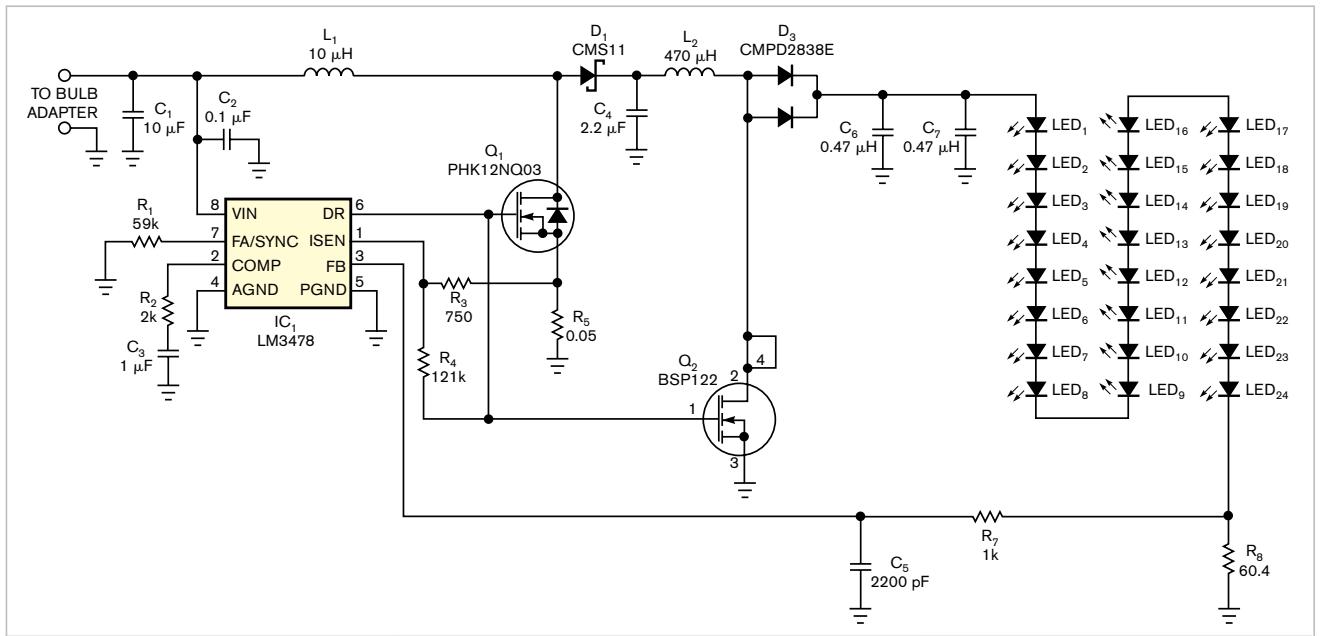
Figure 1 Comprising off-the-shelf components, this circuit cascades two stages of boost to drive a string of 20 to 30 LEDs.

a maximum of about 82% just before the occurrence of undervoltage shutdown. At a normal 4.5V-dc input, the duty factor should be slightly more than 77%.

The circuit in **Figure 1** implements a cascaded boost converter, which takes the place of the lens assembly in a popular heavy-duty flashlight. It includes 24 white or ultraviolet LEDs on one side of the circular PCB (printed-circuit board) and the active circuitry on the other. You can substitute red LEDs for three or four of the ultraviolet LEDs to offer an appropriate visible backlight. Although you may prefer to use a single high-powered white LED, high-powered ultraviolet LEDs appear to be unobtainable. This project uses 20 inexpensive LEDs offering 400 mW of optical power for 1.52W input at a more useful 30° viewing angle. Its directional nature also helps prevent ac-

cidental eye damage. Ultraviolet-light sources find use in many applications, including gem inspection, currency inspection, and scorpion detection.

The PWM controller, IC_1, an LM3478, operates at voltages as low as 3V dc, eliminating the need for a charge pump. The transistors are rated for less than 3V gate drive. IC_1 simultaneously drives Q_1 and Q_2. The circuit requires only one controller and uses off-the-shelf inductors. The first-stage inductor and filter capacitor can produce substantial ripple without adversely affecting the final output ripple. The first rectifier is an inexpensive, 40V Schottky unit, and the second is a simple signal diode rated for 120V.

IC_1 operates at a switching frequency of approximately 300 kHz, which R_1 sets. The design uses a current-mode-control scheme with slope com-

pensation. A signal from current-sense resistor R_5 modulates slope compensation through R_3. In this case, the value of R_5 is small for enhanced efficiency. R_4 sums the signal with the gate-drive output to increase its apparent amplitude by the current-sense input at Pin 1. R_2 and C_3 are the usual compensation components. In this case, the response time of the converter is unimportant, so it is easy to choose the components.

It is easy to overlook the cascaded boost converter without sufficiently analyzing it. Mass-produced components that suit their function afford a more cost-effective and simple approach than you might realize at first. An integrated flyback regulator can easily require many components to provide this kind of solution without any real advantage. It is also likely to require custom magnetics.**EDN**

Dual transistor improves current-sense circuit

Robert Zawislak, PE, Consultant, Palatine, IL

In multiple-output power supplies in which a single supply powers circuitry of vastly different current draws, two perplexing steps are

sensing the current that each output draws and deactivating the power supply in the event of an overload on that output. These issues are especially important in protecting the fragile PCB (printed-circuit-board) traces in low-level circuits. A typical circuit would use the base-emitter threshold volt-

age of approximately 0.6V of a bipolar transistor to trigger the power-supply-protection circuits. Although economical, the transistor's threshold varies excessively over temperature; hence, the protection level is unstable.

The circuit in **Figure 1** essentially eliminates the base-emitter-voltage temperature-variation problem as the derivation of the output voltage and as a function of the load current. By using dual bipolar devices in one case, the manufacturer nearly perfectly matches the two devices. Although this Design Idea describes a positive power supply, you can realize a similar negative-output-supply current-sense circuit using a dual NPN transistor in place of the dual PNP that the **figure** shows.

The following **equations** show the derivation of the output voltage as a function of the load current (referring to **Figure 1**):

$$V_{BA}+(I_{LOAD}\times R_{SENSE})+(I_E\times R_2)-V_{BB}=0.$$
$$[(V_{BA}-V_{BB})+(I_{LOAD}\times R_{SENSE})]-I_E R_2=0.$$
$$I_C+I_B=I_E.$$
$$(V_{BA}-V_{BB})+(I_{LOAD}\times R_{SENSE})-(I_C+I_B)R_2=0.$$
$$I_B=I_C/\beta.$$
$$V_{BA}-V_{BB}+I_{LOAD}\times R_{SENSE}-(I_C+I_C/\beta)R_2=0.$$
$$V_{BA}-V_{BB}+I_{LOAD}\times R_{SENSE}-$$
$$[I_C\times(\beta+1)/\beta]R_2=0.$$
$$V_{OUT}=I_C R_3.$$
$$I_C=V_{OUT}/R_3.$$
$$V_{BA}-V_{BB}+I_{LOAD}\times R_{SENSE}-$$
$$(V_{OUT}/R_3)(\beta+1/\beta)R_2=0.$$
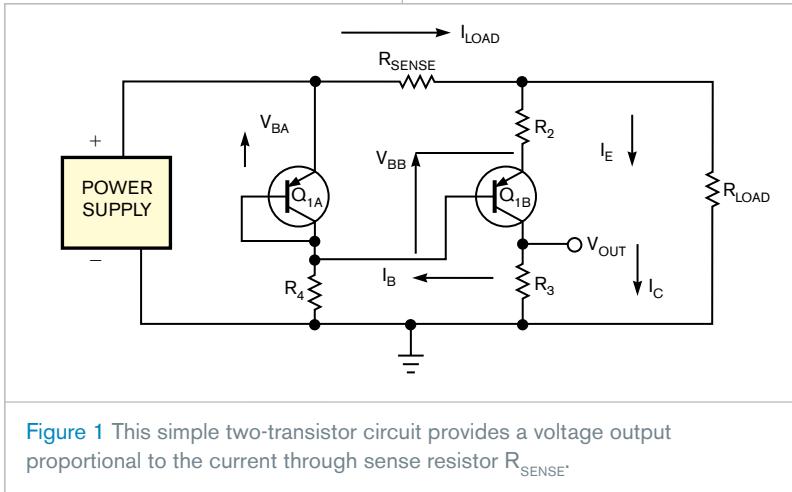If $V_{BA}=V_{BB}$, then $V_{BA}-V_{BB}=0$, and
$$I_{LOAD}\times R_{SENSE}-(V_{OUT}/R_3)(\beta+1/\beta)R_2=0.$$
$$V_{OUT}=I_{LOAD}\times R_{SENSE}[R_3/(\beta+1)](\beta/R_2).$$
If β is high, then $\beta/(\beta+1)\beta)\approx1$, and
$$V_{OUT}=(I_{LOAD}\times R_{SENSE}\times R_3)/R_2.\textbf{EDN}$$

Figure 1 This simple two-transistor circuit provides a voltage output proportional to the current through sense resistor R_{SENSE}.